

1703 E. Highway 50 Yankton, SD 57078 USA Phone: 800-762-8800 or 605-665-9321 Fax: 605-665-1709

Website: www.mtronpti.com



# SPECIFICATION FOR 2.5 x 2.0 mm HCMOS COMPATIBLE SMT OSCILLATOR MtronPTI Part Number M2500S037

### **Electrical Specifications:**

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Frequency of Operation	Fo		13.333000		MHz	
		F	requency Stat	oility		
Frequency Stability	ΔF/F	-100		+100	ppm	Initial frequency @ +25°C, deviation over operating temperature range, shock, vibration, supply voltage, output load, and 1 year aging
			Output			
Output Type		Н	CMOS Compat	tible		
Output Load				15	pF	
Symmetry (duty cycle)	T <sub>DC</sub>	45	50	55	%	Ref to ½ V <sub>DD</sub>
Logic "1" Level	Vон	90% V <sub>DD</sub>			V	HCMOS load
Logic "0" Level	Vol			10% V <sub>DD</sub>	V	HCMOS load
Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>			5	ns	From 10% to 90% V <sub>DD</sub>
Start-Up Time				10	ms	
Trintata Franctica		Logic (70% Vdd min) or floating				Pad 1: Enables output
Tristate Function		Logic (30%	Vdd max) to a	high-Z state		Pad 1: Disables output
Supply Voltage & Power Consumption						
Operating Voltage	$V_{DD}$	3.135	3.300	3.465	V	
Operating Current	I <sub>DD</sub>			8	mA	_

## **Environmental & Mechanical Requirements:**

Operating Temperature	T <sub>A</sub>	-40		+105	°C	
Storage Temperature	Ts	-55		+125	°C	
Mechanical Shock	Per MIL-S	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)				
Vibration	Per MIL-S	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)				
Thermal Cycle	Per MIL-STD-883, Method 1010, B (-55°C to 125°C, 15 min. dwell, 10 cycles)					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 <sup>-8</sup> atm cc/s of Helium)					
Solderability	Per EIAJ-STD-002					
Max. Soldering Conditions	See solder profile, Figure 1					
Package Type	2.0 X 2.5 X 0.9 mm, 4-pad leadless ceramic. RoHS 6/6 compliant					



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#### Dimensions, Marking, and Pin Out Information:

	Pad	Function		Par	t Marking			Legend	
	1	Tristate		Line 1	13M333		у	Year	
	2	Ground		Line 2	M ywwv		ww	Work week	
	3	Output				L	V	Factory code	
	4	+V <sub>DD</sub>							
3   4   DENG	2 0.0983	9 ±0.004 0 ±0.10] =	0.035 [0.9] MAX 0.031	11	in in	TYP	 _ ns n]	ESTED SOLDER PA 0.049 [ 0.031 HH 0.06 HH 0.06	1.25]

Note: Layout should include 0.01 µF or larger capacitor between +Vdd and ground.

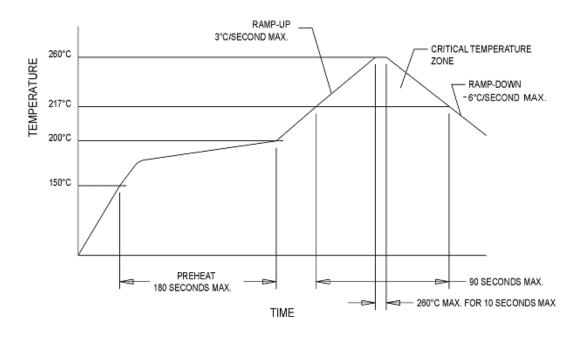


Figure 1

#### **DATA SHEET REVISION TABLE:**

Date	Rev.	Author	Details of Revision
04/15/16	0	DCO	Original Release