





FEATURES

APPLICATIONS

CMOS Output Low RMS Jitter Performance 12 kHz to 20 MHz (1 ps max, 156.25 MHz) RoHS 6/6 Compliant Base station controllers Ethernet Test and Measurement

Ordering Information:

Product Family (Supply Voltage Option)	Temperature Range		Stability		Enable/Disable		Logic Type		Package/Lead Configuration		Frequency MHz
	Code	Value	Code	Value	Code	Value	Code	Value	Code	Value	
M2700 (3.3V) M2701 (2.5V)	6 2	-20 °C to +70 °C -40 °C to +85 °C	3 4 6 8	±100 ppm ±50 ppm ±25 ppm ±20 ppm	Т	Enable High (pad 1)	С	CMOS 45/55	N	Leadless	XXX.XXXXXX
Example: M270024TCN 100.000000 MHz M2700											

Electrical Specifications:

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Frequency of Operation	Fo	10		250	MHz	
		Free	quency Sta	ability		
Frequency Stability	∆F/F		See ordering	g information		
Aging			±2		ppm	1 st year
			RF Outpu	t		
Output Type		CN	IOS Compa	tible		
Output Load		15	pF CMOS I	oad		
Symmetry (duty cycle)		45		55	%	Ref. to 50% Vdd
Logic Level "0"	V _{OL}			10% Vdd	V	
Logic Level "1"	V _{OH}	90% Vdd			V	
Rise/Fall Time	T_R/T_F			5	ns	10% Vdd to 90% Vdd
Start-up Time	T _{SU}			10	ms	$T_{ambient} = +25^{\circ}C$
Enable Logic (Pad 1)		70% V _{CC} or N/C			V	Output Enabled
Disable Logic (Pad 1)				30% V _{CC}	V	Output Disabled to high-Z
	S	upply Voltag	ge & Powe	r Consumpti	on	
Operating Voltage	V _{CC}	3.135	3.300	3.465	V	(M2700)
		2.375	2.500	2.625	V	(M2701)
Supply Current	I _{cc}			60	mA	

Revision B 10/09/17



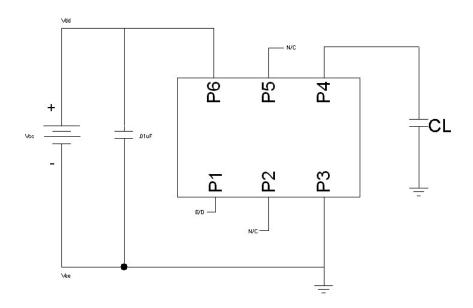




Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125°C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms)
Vibration	Per MIL-STD-202, Method 204D, Condition C (10 g's, 55 – 2000 Hz)
Aging	+85°C ±3°C, 720H (No BIAS)
Humidity	+40°C ±2°CX90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55 °C to +125 °C, 10 cycles)
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻⁸ atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 µm maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.

Typical CMOS Test Circuit & Load Circuit Diagrams:









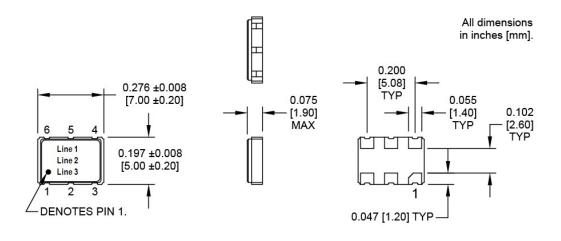
Marking, Pin Out:

Pad	Function					
1	Enable/Disable					
2	No Connection					
3	Ground					
4	Output					
5	No Connection					
6	+V _{cc}					

Part Marking						
Line 1 [part designation						
Line 2	FFFMFFFF					
Line 3	M yy ww vv					

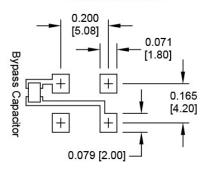
Legend						
M	MtronPTI					
F	Frequency					
уу	Year					
ww	Work Week					
VV	Factory code					

Dimensions:



SUGGESTED SOLDER PAD LAYOUT 4-PAD FOOTPRINT

0.079 [2.00]

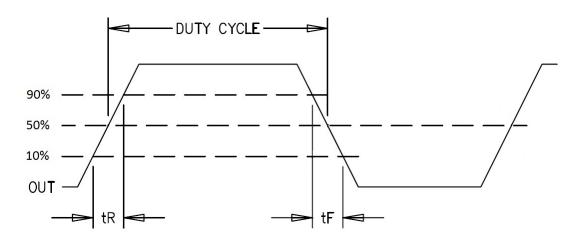








Output Waveform:



Soldering Conditions:

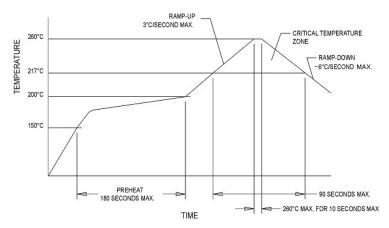


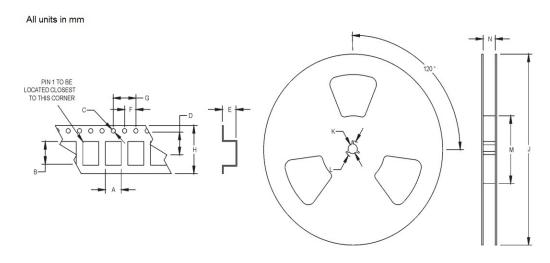
Figure 1







Tape and Reel Specifications:



Tape and Reel Specifications												
Α		В	С	D	Е	F	G	Н	J	K	L	М
^	.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80